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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/821,160	ANDERSON ET AL.	
	Examiner	Art Unit	
	Saqib J. Siddiqui	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-13 and 15-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-13 and 15-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/25/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant's response was received and entered May 16, 2007.

- Claims 1-20 are pending.
- Claims 1, 2, 13, 19 & 12 are amended.
- Application is currently pending.

Response to Amendment

Applicant's arguments and amendments with respect to claims 1-20 filed May 16, 2007 have been fully considered but they are not persuasive. The Examiner would like to point out that this action is made final (See MPEP 706.07a).

Applicant contends that the prior arts of record does not teach utilizing all potential system functional paths and all system clocks on device under test and checking the results by sending the identified last switching latch to a Physical Failure Analysis system. Examiner respectfully disagrees.

The Examiner would like to respectfully direct Applicants attention to page 197 of Sarrica where the reference teaches "the TCM operating in LSSD Scan Mode, verifies that **all** of the SRL's can make all possible transitions (page 197)." By testing all SRL's Sarrica is inherently utilizing all functional paths. Further, there are various scan clocks (A and B), which are both being utilized and given the broadest possible interpretation of the claim limitation "systems clock" scan clocks can be called system clocks. Therefore, Sarrica is in fact utilizing all system clocks and using system clocks to

capture data. Further support for this contention can be taken from Applicant's specification paragraph [0021], where it is mentioned that the data can be output using either system clocks or scan clocks in fact scan clock B is the system clock C2.

It is well known in the art that scan testing incorporates loading, unloading and comparison of data repeatedly. Further evidence of this identifying the last switching latch and a Physical Failure Analysis system can be seen in both the prior arts of records: "...applying enough scan clock cycles to load data into all of the latches...The SRL's are then unloaded using the shift register configuration again... If the actual data matches the predicted data, then the part passes the test." (Sarrica, column 2). "If a part fails one of the scan path tests, automated diagnostics attempts to locate the defect and generate a repair call." (Sarrica, column 3). "The scan ring outputs are connected to TCM output pins such that the data is sent back out to the tester for evaluation." (Sarrica, column 3). "The address stepper SRL's supply the addresses for the arrays. All array locations must be written to when the arrays are being initialized." (Sarrica, column 5). "As an added benefit, it is also sometimes possible to detect latches with extraordinarily slow switching speed." (Sarrica, column 6). Evidence for identifying the last latch and localizing the defect is provided: "Diagnostic software can then count back through the channel data to determine which SRL is stuck, thereby finding the location." (Sarrica, column 8). "An example demonstrating the need for multiple patterns is given..." (Sarrica, column 9). It can be seen that Sarrica teaches loading and unloading data. It mentions that multiple patterns can be used. Further since each

SRL has a corresponding address, which under testing condition is sent to Diagnostic Software. Hence, Sarrica teaches all of the above-mentioned limitations.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sarrica et al. (hereinafter Sarrica) enclosed NPL (Theory and Implementation of LSSD Scan Ring & STUMPS Channel Test and Diagnosis), and further in view of Rajski US Pat no. 6,662,327 B1.

As per claim 1:

Sarrica substantially teaches a method for implementing deterministic based broken scan chain diagnostics (Figure 5) using a computer test system connected to a Physical Failure Analysis system comprising the steps of: generating a deterministic test pattern (Figure 3 "PRPG"); utilizing all potential system functional paths and all system

clocks on a device under test (page 197), loading the test pattern into each scan chain in a device under test using lateral insertion via system data ports and applying system clocks (page 198, Figure 6); unloading each scan chain and identifying a last switching latch in each scan chain (page 198,column 2); repeating the generating, loading, and unloading testing steps a selected number of times (page 199, column 1); and checking for consistent results of the identifies last switching latch in each scan chain (page 199, column 1); and responsive to consistent results being identified, sending the identified last switching latch in each scan chain to said Physical Failure Analysis system to localize a physical defect (page 198, "Diagnostic software").

Sarrica does not explicitly teach the generation of the test pattern to be deterministic.

However, Rajski, in an analogous art, teaches a test generator that generates deterministic test patterns to test circuits under test, including scan chains (column 5, lines 45-66). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to allow Sarrica's invention to be able to test the can chain using deterministic, since one with ordinary skill in the art would have realized that enabling the invention to test with deterministic test patterns accounts for better fault coverage and enables the device to target random pattern-resistant faults. Further it should be noted that the combination of a pseudo random generator with an ATPG (generator of deterministic test patterns) was well-known in the art, at and before the time the invention was made, and was presented in the 'B. Chinaman in "LFSR-Coded Test Patterns for Scan Designs," Proceedings of European Test Conference, pp.237-

242, 1991, this approach combines the benefit of pseudorandom and deterministic patterns' (column 3).

As per claim 2:

Sarrica/Rajski substantially teaches the method as rejected in claim 1 above, further including the steps responsive to consistent results not being identified, of selecting another test pattern; and repeating the testing steps a selected number of times (page 199).

Sarrica does not explicitly teach the generation of the test pattern to be deterministic.

However, Rajski, in an analogous art, teaches a test generator that generates deterministic test patterns to test circuits under test, including scan chains (column 5, lines 45-66). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to allow Sarrica's invention to be able to test the can chain using deterministic, since one with ordinary skill in the art would have realized that enabling the invention to test with deterministic test patterns accounts for better fault coverage and enables the device to target random pattern-resistant faults. Further it should be noted that the combination of a pseudo random generator with an ATPG (generator of deterministic test patterns) was well-known in the art, at and before the time the invention was made, and was presented in the 'B. Chinaman in "LFSR-Coded Test Patterns for Scan Designs," Proceedings of European Test Conference, pp.237-242, 1991, this approach combines the benefit of pseudorandom and deterministic patterns' (column 3).

As per claim 4:

Sarrica/Rajski substantially teaches the method as rejected in claim 1 above.

Sarrica does not explicitly teach the generation of a test pattern wherein the step of generating a deterministic test pattern includes the steps of using perturbations of one base deterministic test pattern from a base deterministic test pattern set generated by an Automatic Test Pattern Generation (ATPG) system.

However, Rajski, in an analogous art, teaches the generation of a test pattern wherein the step of generating a deterministic test pattern includes the steps of using perturbations of one base deterministic test pattern from a base deterministic test pattern set generated by an Automatic Test Pattern Generation (ATPG) system (Figure 4 # 74, column 7, lines 35-60). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to allow Sarrica's invention to be able to generate the deterministic test patterns using perturbations of a base deterministic test pattern, since one with ordinary skill in the art would have realized that enabling the invention to test with perturbations of the base deterministic test patterns would allow the invention to generate a variety of test patterns using minimal resources accounting for better fault coverage (column 7, lines 26-31). Further it should be noted that the combination of a pseudo random generator with an ATPG (generator of deterministic test patterns) was well-known in the art, at and before the time the invention was made, and was presented in the 'B. Chinaman in "LFSR-Coded Test Patterns for Scan Designs," Proceedings of European Test Conference, pp.237-242, 1991, this approach combines the benefit of pseudorandom and deterministic patterns' (column 3). Hence,

the method of generating perturbations of base test patterns falls under the workable range of the invention and it has been held where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233.

As per claim 5:

Sarrica/Rajski substantially teaches the method as rejected in claim 4 above.

Sarrica does not explicitly teach perturbations wherein the step of using perturbations of one base deterministic test pattern includes the steps of applying said one base deterministic test pattern from the base deterministic test pattern set to an exclusive OR and multiplexing a selected perturbation matrix entry using said exclusive OR.

However, Rajski, in an analogous art, teaches perturbations wherein the step of using perturbations of one base deterministic test pattern includes the steps of applying said one base deterministic test pattern from the base deterministic test pattern set to an exclusive OR and multiplexing (Figure 6 # 84) a selected perturbation matrix entry using said exclusive OR (Figure 4 # 78, column 7, lines 35-60). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to allow Sarrica's invention to create perturbations exclusive OR and multiplexing since one with ordinary skill in the art would have realized that enabling the invention to test with perturbations of the base deterministic test patterns would allow the invention to generate a variety of test patterns using minimal resources accounting for better fault coverage (column 7, lines 26-31). Further it should be noted that the combination of a

pseudo random generator with an ATPG (generator of deterministic test patterns) was well-known in the art, at and before the time the invention was made, and was presented in the 'B. Chinaman in "LFSR-Coded Test Patterns for Scan Designs," Proceedings of European Test Conference, pp.237-242, 1991, this approach combines the benefit of pseudorandom and deterministic patterns' (column 3). Hence, the method of generating perturbations of base test patterns falls under the workable range of the invention and it has been held where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233.

As per claim 6:

Sarrica/Rajski substantially teaches the method as rejected in claim 5 above.

Sarrica does not explicitly teach perturbations, including the steps of providing a perturbation matrix with a plurality of perturbation matrix entries including selected ones of no invert, all invert, a predefined bit invert; rotate, and invert rotate.

However, Rajski, in an analogous art, teaches including the steps of providing a perturbation matrix with a plurality of perturbation matrix entries including selected ones of no invert, all invert, a predefined bit invert; rotate, and invert rotate (columns 7-8, lines 64-11). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to allow Sarrica's invention to create perturbations including selected inversions since one with ordinary skill in the art would have realized that enabling the invention to selectively invert would prevent the application of illegal states which could damage the circuit (column 7, lines 64-66). Further it should be

noted that the combination of a pseudo random generator with an ATPG (generator of deterministic test patterns) was well-known in the art, at and before the time the invention was made, and was presented in the 'B. Chinaman in "LFSR-Coded Test Patterns for Scan Designs," Proceedings of European Test Conference, pp.237-242, 1991, this approach combines the benefit of pseudorandom and deterministic patterns' (column 3). Hence, the method of generating perturbations of base test patterns falls under the workable range of the invention and it has been held where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233.

As per claim 7:

Sarrica/Rajski substantially teaches the method as rejected in claim 1 above, wherein the step of generating a test pattern includes the steps of using software Pseudo Random Pattern Generator (PRPG) (Figure 4, page 199).

Sarrica does not explicitly teach the generation of the test pattern to be deterministic.

However, Rajski, in an analogous art, teaches a test generator that generates deterministic test patterns to test circuits under test, including scan chains (column 5, lines 45-66). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to allow Sarrica's invention to be able to test the can chain using deterministic, since one with ordinary skill in the art would have realized that enabling the invention to test with deterministic test patterns accounts for better fault coverage and enables the device to target random pattern-resistant faults. Further it

should be noted that the combination of a pseudo random generator with an ATPG (generator of deterministic test patterns) was well-known in the art, at and before the time the invention was made, and was presented in the 'B. Chinaman in "LFSR-Coded Test Patterns for Scan Designs," Proceedings of European Test Conference, pp.237-242, 1991, this approach combines the benefit of pseudorandom and deterministic patterns' (column 3).

As per claim 8:

Sarrica/Rajski substantially teaches the method as rejected in claim 1 above. Sarrica does not explicitly teach the generation of the test pattern to be deterministic.

Sarrica does not explicitly teach the use of a set deterministic test pattern resident in memory.

However, Rajski, in an analogous art teaches the step of generating a deterministic test pattern including the steps of using a set of deterministic test patterns resident in a memory (Figure 4 # 70, column 7, lines 35-60). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to allow Sarrica's invention to be able to generate patterns from memory, since one with ordinary skill in the art would have realized that enabling the invention to use patterns resident in the memory would allow for an efficient use of resources. Further it should be noted that the combination of a pseudo random generator with an ATPG (generator of deterministic test patterns) was well-known in the art, at and before the time the invention was made, and was presented in the 'B. Chinaman in "LFSR-Coded Test Patterns for Scan Designs," Proceedings of European Test Conference, pp.237-242,

1991, this approach combines the benefit of pseudorandom and deterministic patterns' (column 3).

As per claim 9:

Sarrica/Rajski substantially teaches the method as rejected in claim 1 above, wherein the step of loading the test pattern into each scan chain in the device under test using lateral insertion via system data ports and applying system clocks includes the steps of applying values of the test pattern to selected one of scan chain inputs and primary inputs (Sarrica, page 198).

Sarrica does not explicitly teach the generation of the test pattern to be deterministic.

However, Rajski, in an analogous art, teaches a test generator that generates deterministic test patterns to test circuits under test, including scan chains (column 5, lines 45-66). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to allow Sarrica's invention to be able to test the can chain using deterministic, since one with ordinary skill in the art would have realized that enabling the invention to test with deterministic test patterns accounts for better fault coverage and enables the device to target random pattern-resistant faults. Further it should be noted that the combination of a pseudo random generator with an ATPG (generator of deterministic test patterns) was well-known in the art, at and before the time the invention was made, and was presented in the 'B. Chinaman in "LFSR-Coded Test Patterns for Scan Designs," Proceedings of European Test Conference, pp.237-

242, 1991, this approach combines the benefit of pseudorandom and deterministic patterns' (column 3).

As per claim 10:

Sarrica/Rajski substantially teaches the method as rejected in claim 1 above, wherein the step of loading the deterministic test pattern into each scan chain in the device under test using lateral insertion via system data ports and applying system clocks includes the steps of applying values of the test pattern to selected one of scan chain inputs and primary inputs of latches within each scan chain (Sarrica, page 198).

Sarrica does not explicitly teach the generation of a test pattern wherein the step of generating a deterministic test pattern includes the steps of using perturbations of one base deterministic test pattern from a base deterministic test pattern set generated by an Automatic Test Pattern Generation (ATPG) system.

However, Rajski, in an analogous art, teaches the generation of a test pattern wherein the step of generating a deterministic test pattern includes the steps of using perturbations of one base deterministic test pattern from a base deterministic test pattern set generated by an Automatic Test Pattern Generation (ATPG) system (Figure 4 # 74, column 7, lines 35-60). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to allow Sarrica's invention to be able to generate the deterministic test patterns using perturbations of a base deterministic test pattern, since one with ordinary skill in the art would have realized that enabling the invention to test with perturbations of the base deterministic test patterns would allow the invention to generate a variety of test patterns using minimal resources accounting

for better fault coverage (column 7, lines 26-31). Further it should be noted that the combination of a pseudo random generator with an ATPG (generator of deterministic test patterns) was well-known in the art, at and before the time the invention was made, and was presented in the 'B. Chinaman in "LFSR-Coded Test Patterns for Scan Designs," Proceedings of European Test Conference, pp.237-242, 1991, this approach combines the benefit of pseudorandom and deterministic patterns' (column 3). Hence, the method of generating perturbations of base test patterns falls under the workable range of the invention and it has been held where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233.

As per claim 11:

Sarrica/Rajski substantially teaches the method as rejected in claim 1 above, wherein the step of loading the test pattern into each scan chain in the device under test using lateral insertion via system data ports and applying system clocks includes the steps of applying random data from a software Pseudo Random Pattern Generator (PRPG) to scan chain inputs and primary inputs (Figure 4, page 199).

Sarrica does not explicitly teach the generation of the test pattern to be deterministic.

However, Rajski, in an analogous art, teaches a test generator that generates deterministic test patterns to test circuits under test, including scan chains (column 5, lines 45-66). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to allow Sarrica's invention to be able to test the can

chain using deterministic, since one with ordinary skill in the art would have realized that enabling the invention to test with deterministic test patterns accounts for better fault coverage and enables the device to target random pattern-resistant faults. Further it should be noted that the combination of a pseudo random generator with an ATPG (generator of deterministic test patterns) was well-known in the art, at and before the time the invention was made, and was presented in the 'B. Chinaman in "LFSR-Coded Test Patterns for Scan Designs," Proceedings of European Test Conference, pp.237-242, 1991, this approach combines the benefit of pseudorandom and deterministic patterns' (column 3).

As per claim 12:

Sarrica/Rajski substantially teaches the method as rejected in claim 1 above wherein the step of loading the deterministic test pattern into each scan chain in the device under test using lateral insertion via system data ports and applying system clocks (Sarrica, page 198).

Sarrica does not explicitly teach perturbations wherein the step of using perturbations of one base deterministic test pattern includes the steps of applying said one base deterministic test pattern from the base deterministic test pattern set to an exclusive OR and multiplexing a selected perturbation matrix entry using said exclusive OR.

However, Rajski, in an analogous art, teaches perturbations wherein the step of using perturbations of one base deterministic test pattern includes the steps of applying said one base deterministic test pattern from the base deterministic test pattern set to

an exclusive OR and multiplexing (Figure 6 # 84) a selected perturbation matrix entry using said exclusive OR (Figure 4 # 78, column 7, lines 35-60). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to allow Sarrica's invention to create perturbations exclusive OR and multiplexing since one with ordinary skill in the art would have realized that enabling the invention to test with perturbations of the base deterministic test patterns would allow the invention to generate a variety of test patterns using minimal resources accounting for better fault coverage (column 7, lines 26-31). Further it should be noted that the combination of a pseudo random generator with an ATPG (generator of deterministic test patterns) was well-known in the art, at and before the time the invention was made, and was presented in the 'B. Chinaman in "LFSR-Coded Test Patterns for Scan Designs," Proceedings of European Test Conference, pp.237-242, 1991, this approach combines the benefit of pseudorandom and deterministic patterns' (column 3). Hence, the method of generating perturbations of base test patterns falls under the workable range of the invention and it has been held where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233.

As per claims 13 & 15-18:

Claims 13 & 15-18 are directed to an apparatus of the method for implementing deterministic testing of Claims 1-12. Sarrica, and Rajski teach, either alone or in combination as stated above, the method for implementing deterministic testing as set

forth in Claims 1-12. Therefore, Sarrica and Rajski also teach, either alone or in combination as stated above, an apparatus as set forth in Claims 13 & 15-18.

As per claims 19-20:

Claims 19-20 are directed to a computer program of the method for implementing deterministic testing of Claims 1-12. Sarrica, and Rajski teach, either alone or in combination as stated above, the method for implementing deterministic testing as set forth in Claims 1-12. Therefore, Sarrica and Rajski also teach, either alone or in combination as stated above, a computer program as set forth in Claims 19-20.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saqib J. Siddiqui whose telephone number is (571) 272-6553. The examiner can normally be reached on 8:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Saqib Siddiqui
Art Unit 2138
07/10/2007

GUY LAMARRE
PRIMARY EXAMINER